

Notice of References Cited	Application/Control No. 09/754,406	Applicant(s)/Patent Under Reexamination XU, SONGJIE	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,648,913	07-1997	Bennett et al.	716/6
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chen et al., "Combining Technology Mapping and Placement for Delay-Optimization in FPGA Designs" 1993 Unvi. of Tsing Hua IEEE pg.123-127.
	V	Cong et al., "Delay-Optimal Technology Mapping for FPGAs with Heterogeneous LUTs" 1998 ACM pg.704-707.
	W	Murgai et al., "Performance Directed Synthesis for Table Look Up Programmable Gate Arrays" 1991 IEEE pg.572-575.
	X	Changfan et al., "Timing Optimization on Routed Design with Incremental Placement and Routing Characterization" 2000 IEEE pg.188-196.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.